E.ON Energy Research Center | RWTH AACHEN UNIVERSITY

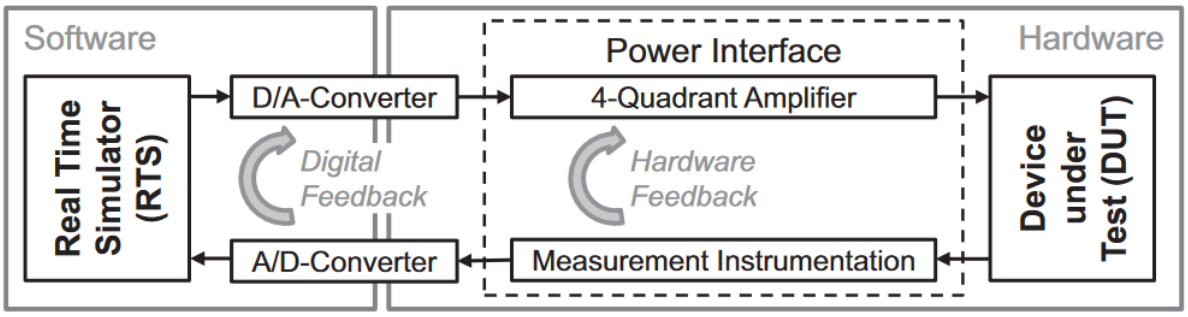
Master-Thesis:

Requirements, design and analysis of Power-Hardware-in-the-Loop application

Context:

The laboratory at the Institute for Automation of Complex Power Systems is equipped with the Digital Real-Time Simulators (DRTSs), OPAL-RT and RTDS, developed for real-time simulations of power systems. One of the main applications of DRTSs is testing and validation of devices based on (Power) Hardware-in-the-Loop (PHiL, HiL) concept. PHiL combines the processes of simulation and hardware testing. A part of the system, that should be investigated, exists as a real hardware while the rest of the system is represented by models in a real-time simulation environment. A battery energy storage system (battery and its inverter) represents device under test (DuT).

Power Hardware-in-the-Loop simulations require interfacing between DuT and DRTS. Signals from the simulator must be amplified and power interface must be provided for DuT. For this purpose power interface called Grid Emulator is developed by Institute for Power Generation and Storage Systems (PGS).



Principal design of a Power-Hardware-in-the-Loop setup

Due to several aspects of PHiL set-up (discretization, D/A and A/D converters, calculation time, grid emulator characteristics etc), PHiL can struggle with both accuracy and stability. Interface algorithm (IA) for PHiL determines which signals are and when those signals are exchanged between real-time simulator and DuT. This thesis is about design and analysis of PHiL interface algorithm, requirements and analysis of PHiL set-up.

Your tasks:

- Modeling of PHIL setup for systematic analysis
- Implementation and analysis of interface algorithms proposed in the literature
- Stability and accuracy analysis of the PHIL setup
- Derivation of requirements for communication interface and grid emulator

References:

S. Hubschneider et al., "Requirements for Power Hardware-in-the-Loop Emulation of Distribution Grid Challenges," 2018 53rd International Universities Power Engineering Conference (UPEC), Glasgow, 2018, pp. 1-6.

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G. F. Lauss, M. O. Faruque, K. Schoder, C. Dufour, A. Viehweider and J. Langston, "Characteristics and Design of Power Hardware-in-the-Loop Simulations for Electrical Power Systems," in IEEE Transactions on Industrial Electronics, vol. 63, no. 1, pp. 406-417, Jan. 2016.

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